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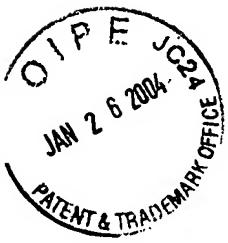
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S/N 10/003,238IN THE UNITED STATES PATENT AND TRADEMARK OFFICEPATENT

Applicants: Carlos A. Gonzalez et al. Examiner: James M. Mitchell
Serial No.: 10/003,238 Group Art Unit: 2827
Filed: October 26, 2001 Docket No.: 884.535US1
Title: ELECTRONIC ASSEMBLIES WITH FILLED NO-FLOW UNDERFILL
Assignee: Intel Corporation Customer No.: 21186

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

This declaration is submitted under 37 C.F.R. §1.131 prior to any final rejection of U. S. Patent Application Serial Number 10/003,238 to establish invention of the subject matter of the rejected claims prior to January 5, 2001.

I, Song-Hua Shi, do hereby declare:

1. I have been employed by Intel Corporation from prior to January 5, 2001 until the present. My current job title is Senior Process Engineer.

2. I am a co-inventor of the inventive subject matter of the present application as described, illustrated, and claimed therein.

3. Prior to January 5, 2001, the inventive subject matter that is described, illustrated, and claimed in corresponding claims of the present application was completed in the United States as evidenced by the following:
 - a. Prior to January 5, 2001, having earlier conceived the claimed subject matter in the United States with the co-inventors, I personally generated a draft of an Invention Disclosure, a copy of which is attached hereto as Exhibit A (8 pages). The dates that have been deleted from Paragraphs 13 and 16 of Exhibit A are prior to January 5, 2001. Other sensitive information has been blocked out from Exhibit A.

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- b. Figure 2 of Exhibit A illustrates conceptually an IC (integrated circuit) die having terminals being attached to corresponding pads of a substrate.

A liquid, low CTE (coefficient of thermal expansion) fluxing no-flow underfill material is dispensed on a component-mounting area of a substrate, including on the substrate pads. Particles of silica filler are shown surrounding one of the substrate pads. This is seen in the illustration in the left-hand side of Figure 2 of Exhibit A, which corresponds to FIG. 5 of the present application.

Following the direction indicated by the first arrow of Figure 2, the next illustration shows an IC with its terminals aligned with and compressed down upon the pads of a substrate, squeezing out particles from between the terminals and the pads. This illustration corresponds to FIG. 6 of the present application. As further described in Exhibit A, e.g. in Paragraph 14, in an embodiment the fluxing capability of the underfill material effectively removes metal oxide from the surface of the interconnect structure, such as terminals, pads, pre-solders, and copper materials, during a soaking period at a temperature ranging from 130-180C.

Following the direction indicated by the second arrow of Figure 2, the next illustration shows the IC with its terminals completely joined to the pads of a substrate, following the application of suitable heat to reflow solder. When cooled, the hardened underfill encapsulates the terminals, pads, and solder connections. This illustration corresponds to FIG. 7 of the present application.

- c. Prior to January 5, 2001, I was personally involved in the construction of prototype IC packages utilizing low CTE fluxing no-flow underfill materials, as described in Exhibit A. My responsibilities included the selection of materials and equipment; defining high-volume, cost-effective processes to improve yield and reliability of IC-to-substrate interconnections using low CTE fluxing no-flow underfill materials; the building and testing of prototypes; and analyzing test results.

- d. Exhibit B (1 page) shows an optical microphotograph of a cross-section of a prior art IC-to-substrate interconnection. I received and analyzed this microphotograph prior to

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January 5, 2001. This interconnection has an underfill material that did not contain any significant amount of low CTE silica particles, and in which compression was not used to press the IC onto the substrate prior to or concurrently with heating. The die is shown in the upper portion of Exhibit B. In this test, the die has a number of relatively high melting point terminals or bumps of hemispherical shape. The substrate, in the lower portion of Exhibit B, has a number of substrate pads, each of which has a relatively low melting point solder bump of roughly hemispherical shape. After subjecting this interconnection to reflow temperature, without added compression, the substrate solder bumps melted, but they did not experience adequate wetting or form good quality solder joints with the corresponding die bumps. A typical example of a poor quality solder joint with poor wetting is shown in the white-outlined box labeled "2 Solder Bumps With Poor Wetting".

e. Exhibit C (1 page) shows an optical microphotograph of a cross-section of an IC-to-substrate interconnection, in accordance with an embodiment of the present application. I received and analyzed this microphotograph prior to January 5, 2001. This interconnection has an underfill material containing low CTE silica particles, which may be seen within the underfill material in the spaces between the solder joints, one example of which is identified by the white-outlined box labeled "Filler Particles". The silica particles were approximately spherical and ranged in size from approximately $0.1\text{ }\mu\text{m}$ to $40.0\text{ }\mu\text{m}$, with an average size of about $10.0\text{ }\mu\text{m}$. The fluxing agent used in the underfill was ester acid, which is an organic carboxylic acid. In addition, compression was provided by a thermocompression bonder to press the IC onto the substrate after the IC reached soaking temperature, in order to squeeze out silica particles. The die is shown in the upper portion of Exhibit C. In this embodiment, prior to reflow temperature, the die had a number of relatively high melting point terminals or bumps of hemispherical shape, and the substrate, seen in the lower portion of Exhibit C, had a number of substrate pads, each of which had a relatively low melting point solder bump of roughly hemispherical shape. After subjecting this interconnection to reflow temperature, while continuing to maintain compression with the thermocompression bonder, the substrate solder bumps melted, experienced good wetting, and formed high quality solder joints with the corresponding die bumps. A typical example of a high quality solder

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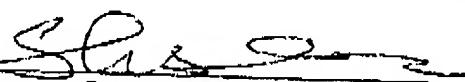
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joint with good wetting is shown in the white-outlined box labeled "High Quality Solder Joint".

f. When I finished testing and evaluating the prototype IC package of the type shown in Exhibit C, I believed that it worked satisfactorily for its intended purpose, by providing a potentially high yield, high reliability component package having a filled, no-flow underfill.

4. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: 1/15/2004


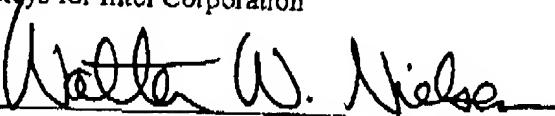
Song-Hua Shi

CARLOS A. GONZALEZ ET AL.

By their Representatives,
 SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
 Attorneys for Intel Corporation

Date 1/16/2004

By



Walter W. Nielsen
Reg. No. 25,539

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage or first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20 day of January, 2004.

Name

KACIA LEE

Signature

Kacia Lee

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TMG INVENTION DISCLOSURE
Located at: <http://legal.intel.com>

LEGAL ID# _____ (legal dept. use only)

DATE: _____

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to Intel Legal Department at JF3-147. You can submit electronically via e-mail to "invention disclosure submission" if all of the information is electronic, including drawings and supervisor approval. If you have any questions regarding this form or to whom it should be forwarded, please call

Fill out the below and follow the instructions:

1. **Field of the Invention:**
 - Semiconductor Process: device and integration
 - Semiconductor Process + Equipment: thin films
 - Semiconductor Process + Equipment: etch/litho
 - Circuit Design
 - Flash
 - Test
 - CQN (Q&R)
 - Packaging
 - Boards/Cartridge
 - Automation
 - Other
2. **Concise Title of Invention:** The process of making electrically conductive structures of flip-chip packages by using fluxing underfill materials

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3. **Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):**

The invention is: a novel process of making electrically conductive structures for fine pitch flip-chip packages by using fluxing no-flow underfill materials. With the help of instant chip joint machine, this process is invented to provide simultaneous chip joint and underfill by using filled or non-filled fluxing underfill materials (no-flow underfill materials). Therefore, the new process can significantly simplify the flip-chip package manufacturing process and reduce manufacturing cycle time and cost.

The key elements are: instant chip joint process powered by fluxing underfill materials.

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4. Inventor(s):

Name: Carlos A. Gonzalez

E-Mail Address:

WWID#

M/S:

Phone: Fax: Home Address:

Citizenship: Supervisor Name: Supervisor Phone: Supervisor M/S:

Group Name: TMG Contractor: Inventor Signature:

Division Name: ATD_X

PTD CTM CR YES _____

STTD CQN _____

SMTD TCAD _____

Other? _____

Name: Song-Hua Shi

E-Mail Address: WWID#

M/S:

Phone: Fax: Home Address:

Citizenship: Supervisor Name: Supervisor Phone: Supervisor M/S:

Group Name: TMG Contractor: Inventor Signature:

Division Name: ATD

PTD CTM CR YES _____

STTD CQN _____

SMTD TCAD _____

Other? MTO _____

Name: Milan Djukic

E-Mail Address: WWID#

M/S:

Phone: Fax: Home Address:

Citizenship: Supervisor Name: Supervisor Phone: Supervisor M/S:

Group Name: TMG Contractor: Inventor Signature:

Division Name: ATD

PTD CTM CR YES _____

STTD CQN _____

SMTD TCAD _____

Other? _____

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

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- 5. HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)**

DATE: _____ SUPERVISOR NAME: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

- 6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date: No
(Give expected tape out date if applicable):**
- 7. Has the subject matter of present disclosure been published or will it be published outside of Intel? No
If yes, explain and give date:**
- 8. Has a product using or manufactured using the present disclosure been sold or offered for sale?
If yes, explain and give date: No**
- 9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number: No**
- 10. Explain the problem being addressed by the invention:**

This invention addresses the problem of: a) low assembly yield by using silica filled no-flow underfill material, b) low reliability by using non-filled no-flow underfill materials, c) complexity and throughput time of current capillary flow underfill d) assembly cost

- 11. Explain current state of the art (i.e., how the problem is solved today):**

Today, we cannot make use of no-flow technology for CPU packages because non-filled materials do not meet the CTE and modulus requirements to make a reliable package. On the other hand, filled no-flow materials (new formulations driven by Intel) cannot be used with the current pick&place and reflow process.

- 12. Explain technical advantages of the invention over current state of the art:**

The technical advantage of this invention is: the use of silica-filled no-flow underfill materials and low CTE no-flow underfill materials is allowed in this invented process with satisfactory interconnection yield. The Interconnection yield is significantly improved due to the low viscosity and fluxing capability of the liquid no-flow underfill material. Moreover, the instant chip join machine can provide reasonably high chip placement force to effectively increase the contact opportunity of bump to pad during chip join process, and therefore further effectively improve the interconnection yield.

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13. a. Is the invention experimentally verified? Yes
b. Is the invention verified with simulation?
c. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

The experimental data will be provided by [REDACTED]

Include x-section images here

The technical basis are as follows:

The fluxing capability in the no-flow underfill materials can effectively remove the metal oxide on the surface of bumps, pads, pre-solders, and copper columns during the soaking period at temperature ranging from 130°C to 180°C to allow good wetting of the substrate solder material to die bump (copper or high lead). The high placement force and low viscosity of the no-flow materials can effectively increase the contact opportunity between bump and pad and facilitate the squeezing out of silica particles in between the bumps and bump-shaped pre-solder pads during solder wetting process. As a result, the interconnection yield is significantly improved. Since the no-flow underfill is heavily silica-filled or low CTE no-flow material, the satisfactory reliability of the assembled packages are also achieved.

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14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

The uniqueness of this invention is the use of liquid silica-filled fluxing no-flow underfill materials or low CTE fluxing no-flow underfill materials. The fluxing capability in the no-flow underfill materials can effectively remove the metal oxide on the surface of bumps, pads, pre-solders, and copper columns during the soaking period at temperature ranging from 130°C to 180°C to allow the quick wetting of solder material to copper and high lead material. The high placement force and low viscosity of the no-flow materials can effectively increase the contact opportunity between bump and pad and facilitate the squeezing out of silica particles in between the bumps and bump-shaped pre-solder pads during solder wetting process. As a result, the interconnection yield is significantly improved. Since the no-flow underfill is heavily silica-filled or low CTE no-flow material, the satisfactory reliability of the assembled packages are also achieved.

In this process (Figure 2), the silica-filled no-flow underfill material or low CTE underfill material is dispensed at the center of bonding pad area on a pre-heated substrate. A chip is then picked-up and heated to soaking temperature, aligned and compressed down to the underfill material. After the chip reaches the position, it is held for sometime (soaking time) to allow the flux to remove the metal oxide. Then, the chip is heated above the melting temperature of the solder while maintaining the placement force. After that, the entire structure is cooled down naturally and may experience post-cure if needed.

Referenced sketches/dwg's/diagrams: (use additional page(s))

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15.

**Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)**

Figure 1. Present State of the Art (often this is helpful to explain your invention, but it is not required).

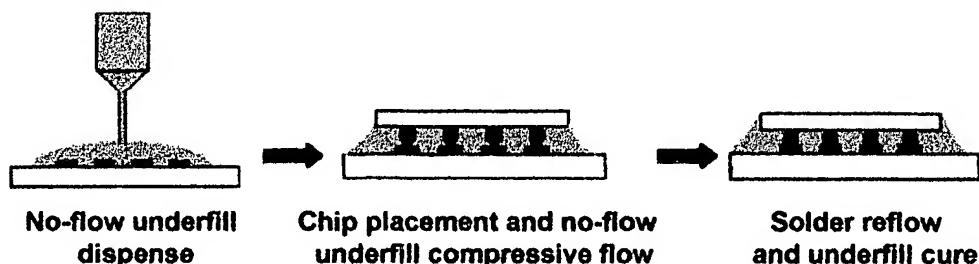


Figure 1 (a): No-flow underfill process

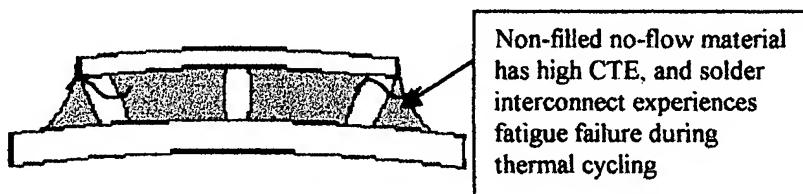


Figure 1 (b): Non-filled no-flow underfill material can not effectively protect solder interconnects

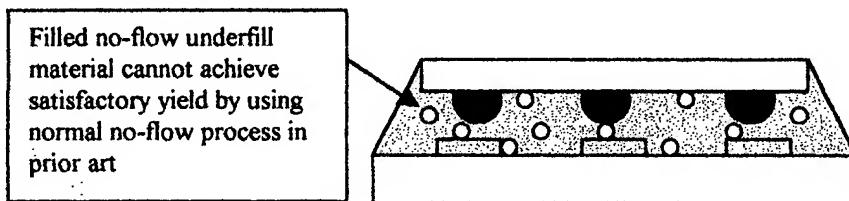
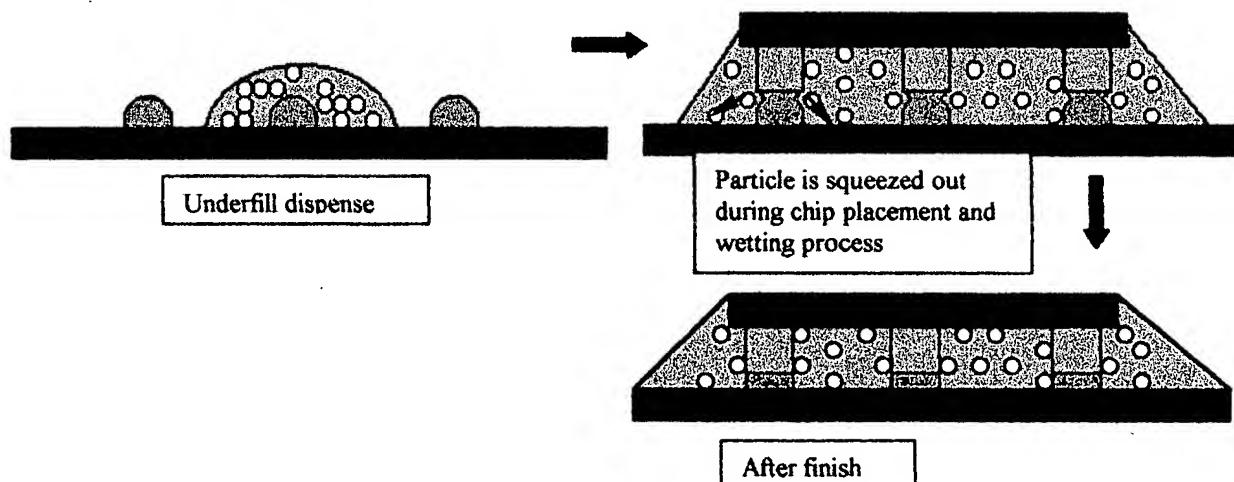


Figure 1 (c): Filled no-flow material significantly reduce interconnection yield by silica inclusion in-between the bump and bonding pad.

Figure 2. The Invention (use additional figures as needed to show details and additional embodiments)



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- 16. Key Supporting Data (1 page limit on separate page):**

Will be provided by [REDACTED]

- 17. What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):**
P1262 and X64 products

- 18. Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name:** _____

- 19. Any other information IP committee should consider? No**

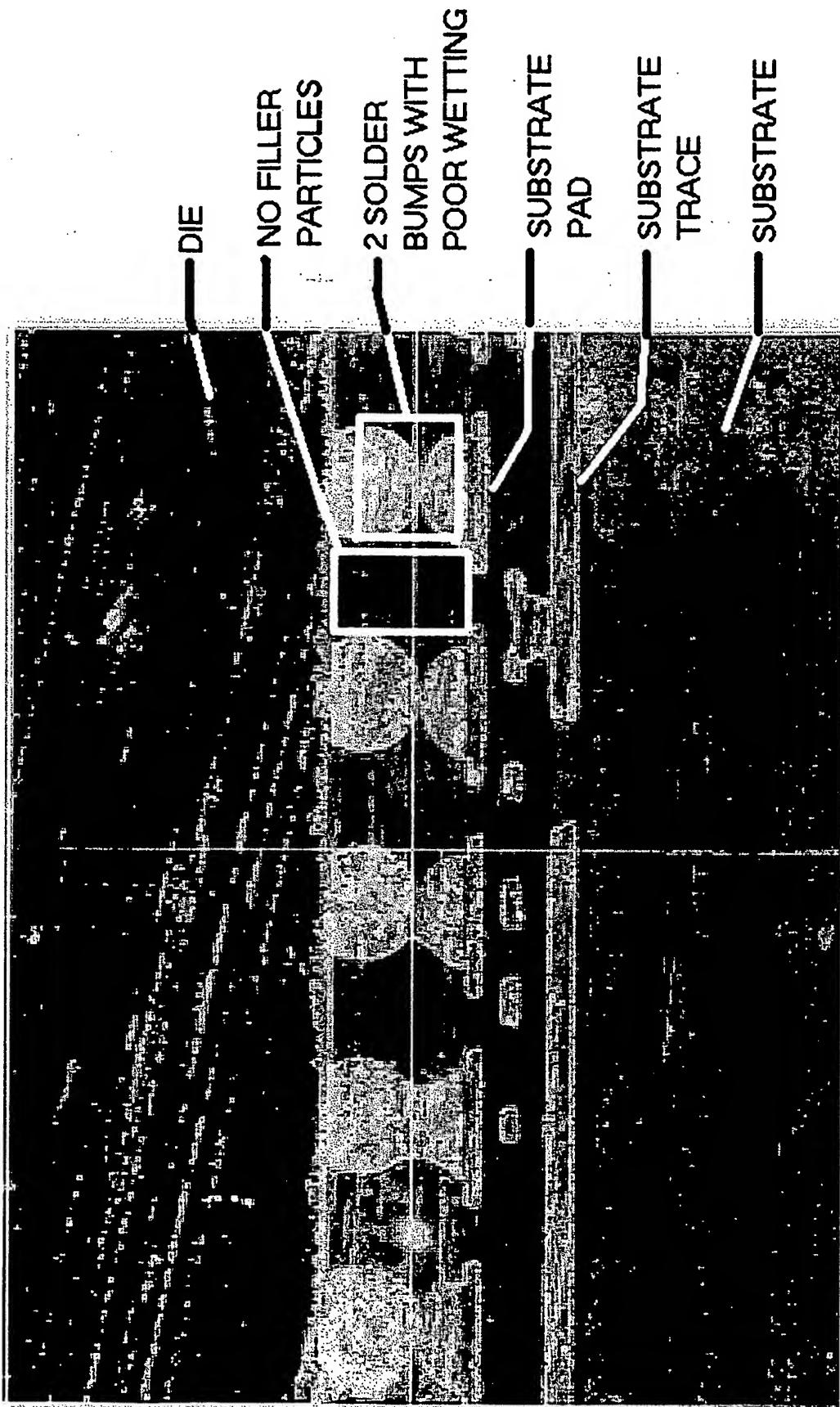


EXHIBIT B

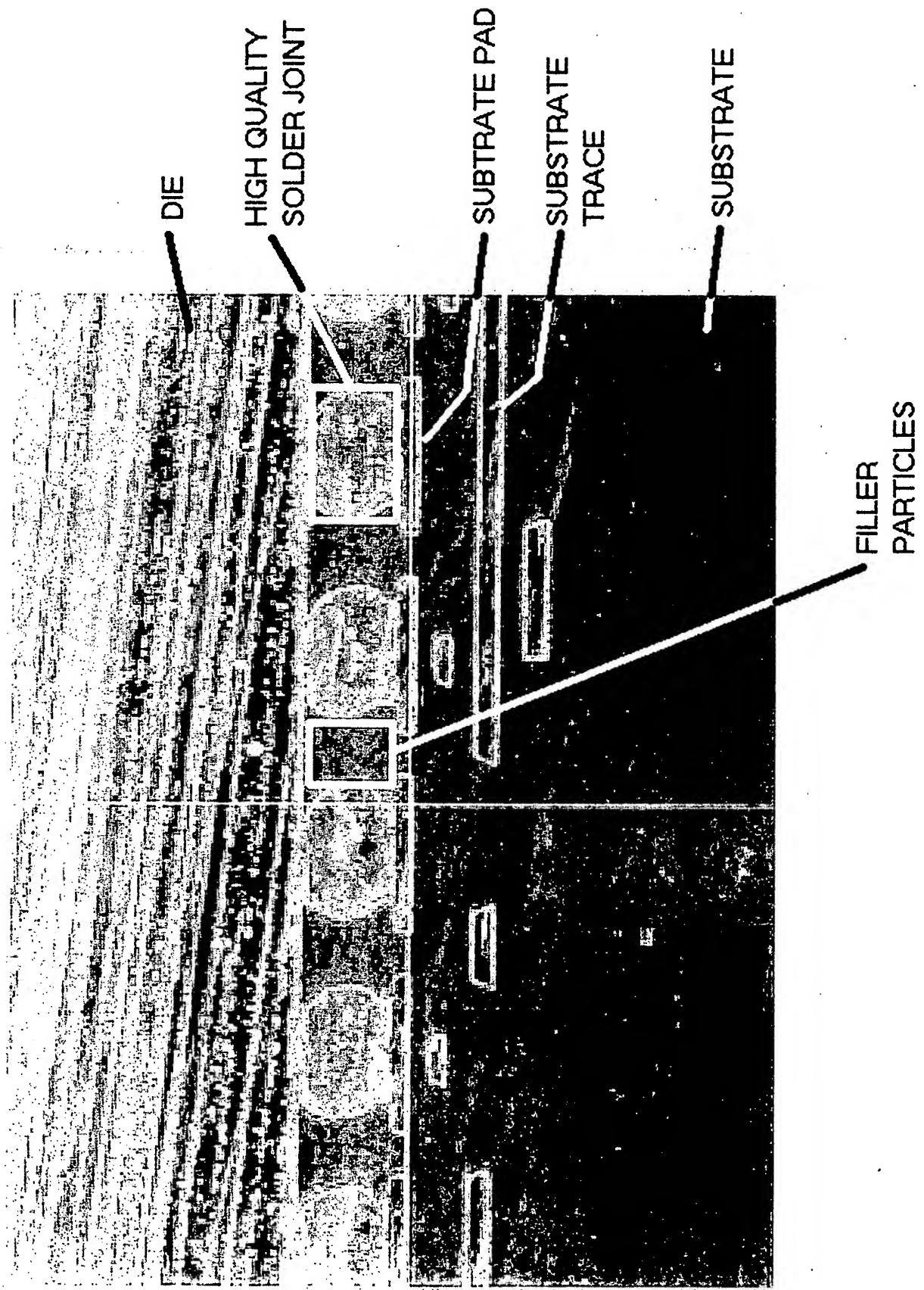


EXHIBIT C